Progress in 0.25μ Pixel FE chip (FE-I)

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Approximate division of effort:

- Who is doing what...

Test Chip Program:

- First TSMC submission in Jan
- Second set of submissions in late Feb (IBM MPW) and early March (TSMC)

Progress towards IBM Engineering Run

Rough Division of Tasks

Front-end and control block design:

- This is a collaboration of Laurent Blanquart and Peter Fischer.

Other analog blocks (reference, LVDS I/O, DACs, Chopper):

- In some cases (reference and LVDS), schematics are done by Laurent and layout by Ivan and Peter in Bonn, in other cases design and layout are done by Bonn.

Digital readout in column and bottom of column

- This includes the hit logic, pixel storage, CEU block, and sense amps. It is being done by Emanuele Mandelli.

End of Column buffers

- This was done by Roberto Marchesini, who has now left LBL. The integration of these blocks with the rest of the chip will be completed by Gerrit Meddeler.

Bottom of chip, digital logic

- This is being done by Gerrit Meddeler

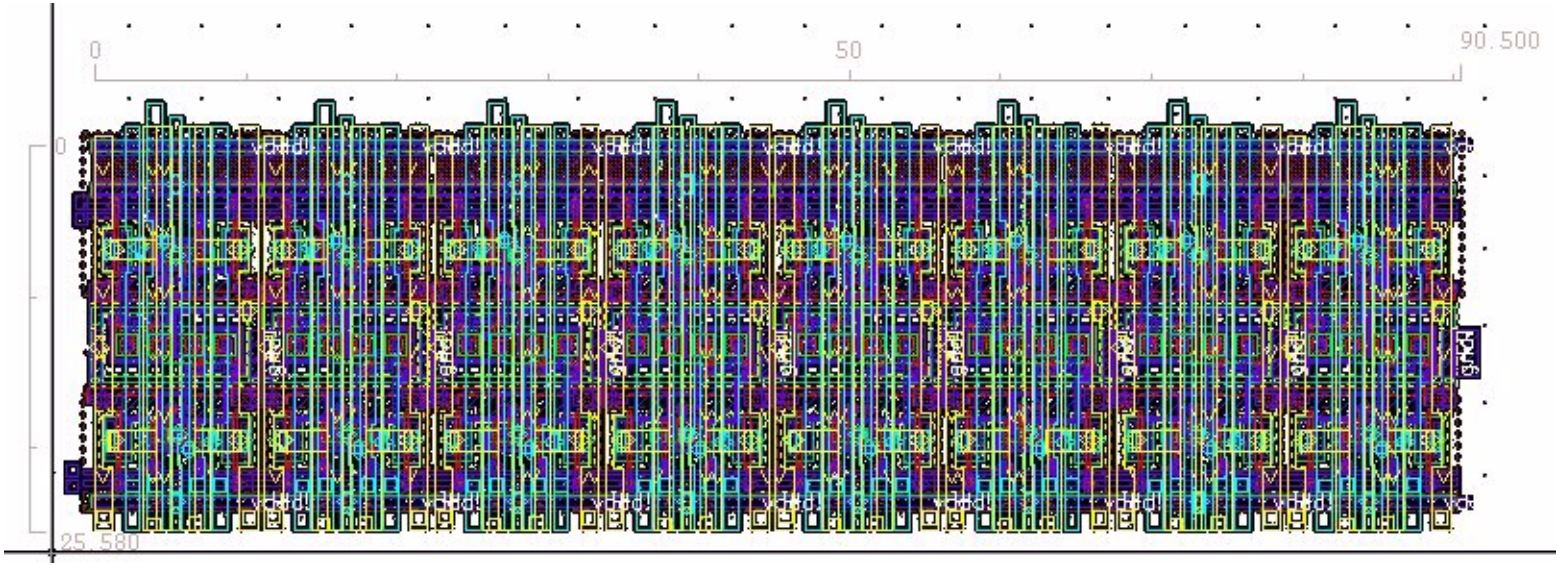
Technology files, pad frame, standard cell library

- This is a collaboration among Peter Denes, Gerrit Meddeler, and Giacomo Comes.

Status of Digital Readout:

RAM cell:

- Completed in Dec for submission in Jan TSMC chip. A new design, using a differential SRAM cell consisting of 8 transistors. The TSI are transmitted differentially, data from the pixel is sent differentially as well. Size for two 8-bit LE/TE RAMs plus 8-bit address ROM is 50µ x 100µ (storage for one pixel shown).

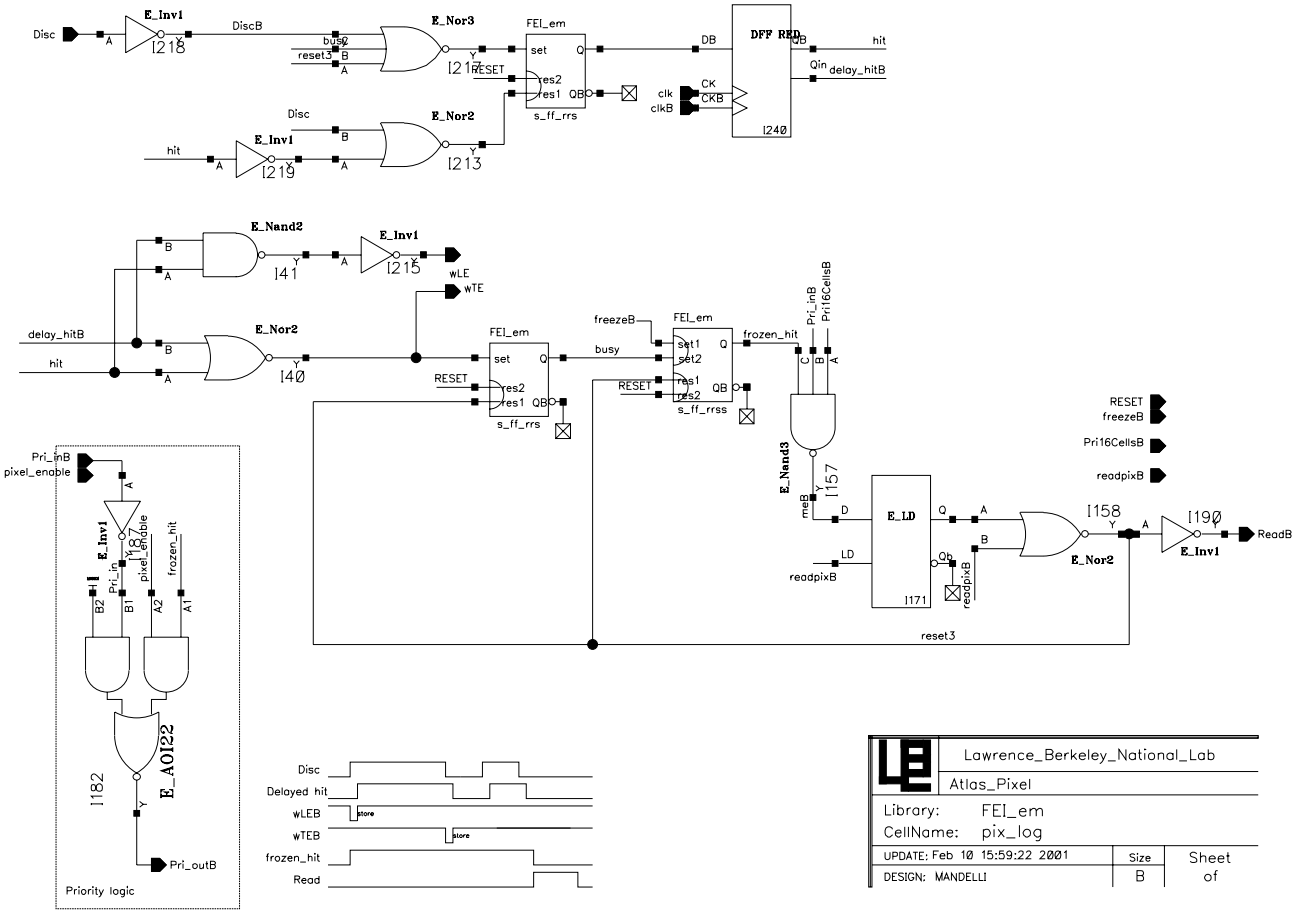


- Note that the use of a static RAM has significant implications for the Hit Logic design. In the old DRAM design, all pixel RAMs were sitting on the TSI bus in transparent mode (which increased the power consumption for TSI distribution). For a static design, it is not possible to be constantly driving against the internal inverters, so the approach has to change. Now, RAMs are only written when there is a hit to write into them.

Hit Logic:

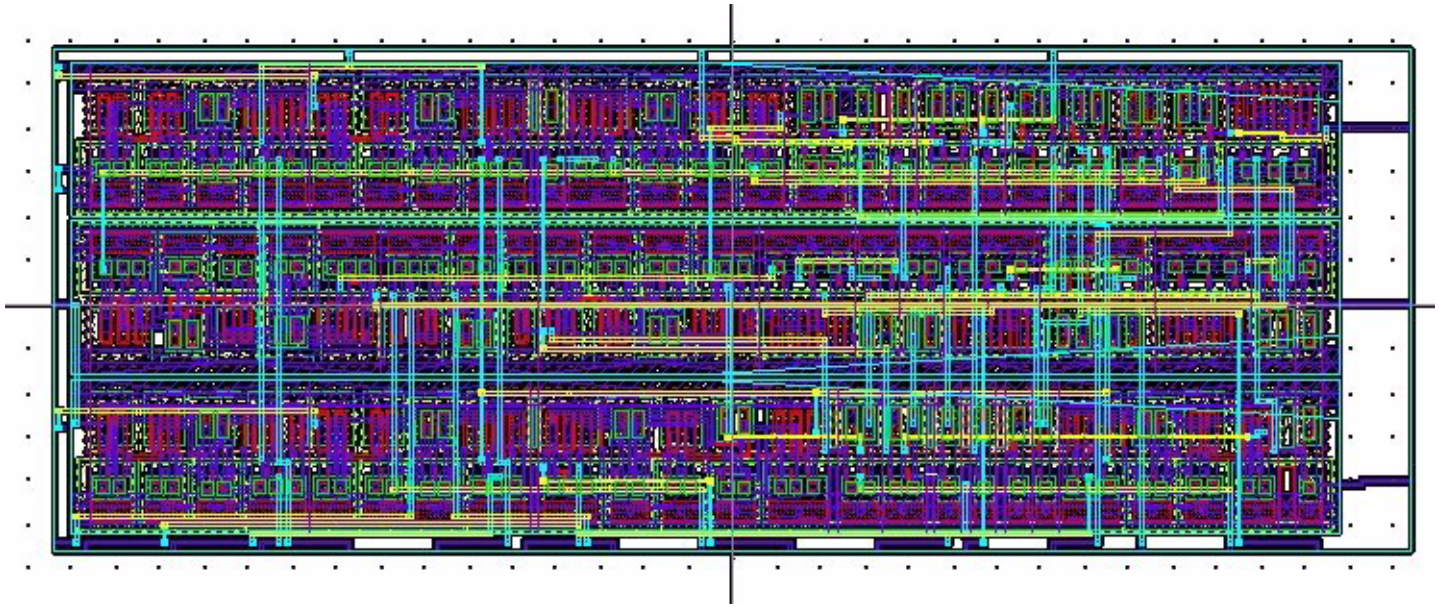
- For the SRAM implementation, it is necessary to generate short WriteLE and WriteTE pulses. They should not be too wide, or variations in their width will increase the timewalk budget. They should not be too narrow, or there is a chance that the RAM will not be written. This was the design intially pursued, using an inverter chain to generate pulses with roughly 1ns width.
- A second approach is to replace the asynchronous write design with a synchronous design, where the writes occur only on XCK edges. In this case, a pulse stretcher must also be included to avoid missing narrow hits that do not overlap a clock edge. The timing is very conservative, because the TSI are incremented on the XCK rising edge, and the RAM write occurs on the falling edge of TSI. The RAM Write pulses are 12.5ns wide. The disadvantage of this design is that it requires two FF per pixel, clocking at 40MHz. Using two large standard cell DFF, this leads to a power consumption of over 100mW just for the FFs. Using an optimized DFF design, the power can be kept below 30mW.
- Further optimization of both approaches is being pursued. For the first design, an adjustable pulse width with a current-starved inverter chain could be included. Further studies of the design margin will also be carried out. For the second design, more optimal DFF designs are being examined to minimize the power consumption. Although it is no longer data-driven, the second design looks more conservative, and hence more promising, at this time.

- Schematic of logic with synchronous Hit writing and low power DFF:



- Another feature introduced is to gate the sparse scan output form each pixel with the ReadoutEnable FF from the control block. Previously, disabling a pixel just meant blocking the discriminator hit from the input to the Hit logic. The new approach is more robust, and would (for example) allow disabling malfunctioning pixels such as those that are common in the FE-D chips.

- Layout for new block was done using Silicon Ensemble for automatic place and route and using the modified RAL standard cell library. It is 50µ x 75µ. The layout below also includes a control block with the same schematic as FE-H, which adds a further 50µ when layed out with standard cells. However, Peter Fischer is now working on new design based on full custom layout (see later).

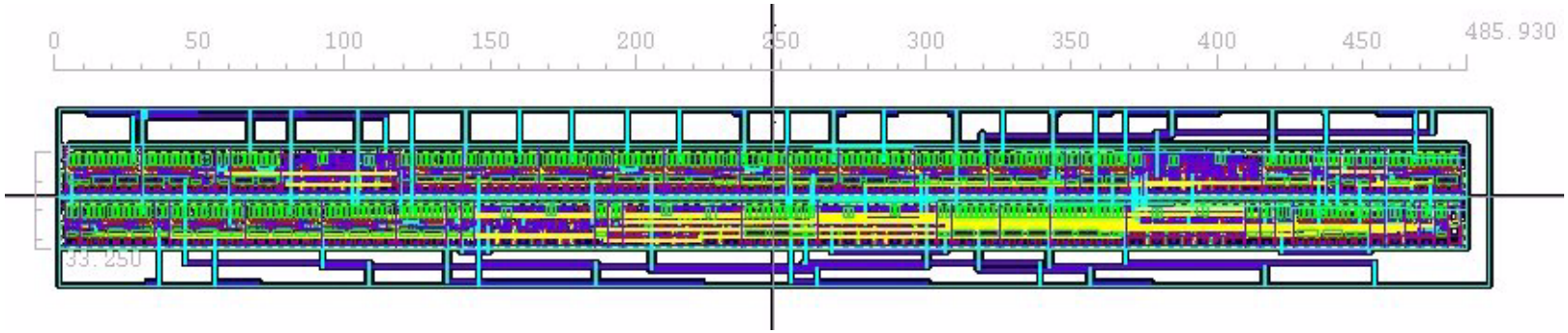


Sense Amps:

- This design was also completed in Dec and included in the TSMC submission. The sense amplifiers are differential, matching the SRAMs in the pixel. The data transmission along the column pair uses voltage-mode transmission with VDD/2 amplitude, but fully differential. This appears to be the best approach for a full CMOS chip (FE-D with bipolar sense amplifiers had lower swing).

CEU Logic:

- The design of this block has been completed for the “no TOT correction” case. For the synchronous write Hit logic design, it is simpler because no ClearPix signal is required. It has also been layed out using P&R with standard cells. The layout, included all appropriately sized buffers for driving the column pair (TSI plus control signals) is roughly 35µ x 500µ, but different aspect ratios can easily be generated as the final floorplan becomes clear:



TOT Correction:

- Peter Fischer proposed the idea of carrying out the TOT calculation in the CEU, and then applying a simple timewalk correction for small pulse height hits. The correction would start with a TOT trim DAC in each pixel to create a uniform charge response throughout the chip. Then, the TOT subtraction logic presently in the bottom of the chip (Gray->Binary conversions for LE and TE data, and modulo subtraction of LE from TE to create digital TOT) would be moved to the CEU. Therefore, the CEU would output LE and TOT information in Binary format.

- Two simple algorithms for using this information would be implemented. For both cases, there would be a TOT Threshold register included in the Global Register. For the first algorithm, this digital threshold would be used to inhibit small pulse height hits from being written into the EOC buffers. For the second algorithm, the hit would be written twice. It would be written once with (LE-1) assuming the hit belonged to an earlier crossing but suffered timewalk, and once with LE.
- A first look at the circuitry required for this suggests that it would be about a 50% increase over the present CEU. More detailed studies are underway, including completing the design, and examining the power consumption increase. Based on these studies, we will decide whether or not to use this block in the FE-I chip.

EOC Buffers:

- A complete state-machine implementation of the EOC Logic block has been implemented. This involves a 4-state machine with no unused states, and bit flips in the state machine lead to only minor transient disruptions.
- The completed block has a size similar to that of the FE-H EOC buffers, and should allow implementing 32 buffers in FE-I with no problems. Perhaps 40 buffers would be possible, which provides a chip with fair good B-layer performance when the column clock is operated at 20MHz.
- First simulations of the EOC buffers connected to the bottom of chip logic are being performed using Verilog, and will be continued at great length...

Bottom of Chip:

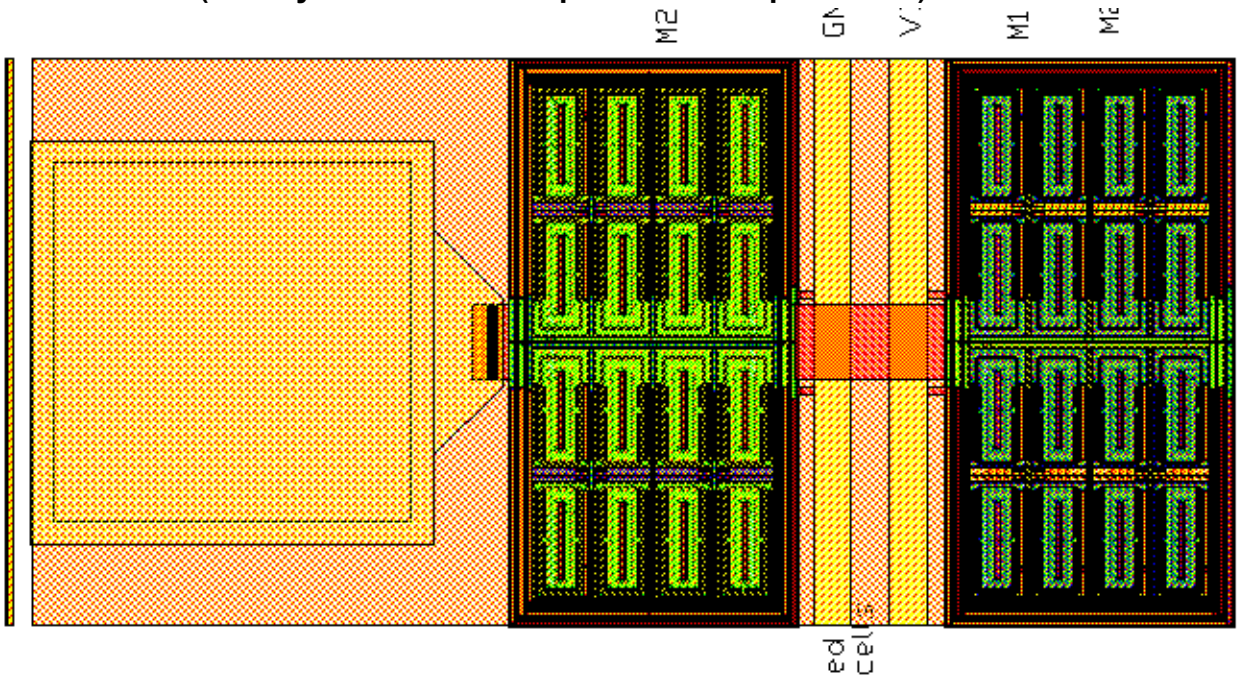
- This logic is largely unchanged from the FE-H version.
- Minor updates have been made to integrate the present EOC Logic design, and more updates might be required for the TOT correction, but they will also be minor.
- Synthesis with Synopsis has been tested, but it is clear that some of the characterization information from RAL is not of high quality. In particular, the corner timing information seems to be wrong, and leads to very large speed variations with corner models. RAL has promised to deliver an update on the timescale of a few weeks.

Standard Cell Library:

- Giacomo Comes has modified the existing RAL library to make it TSMC compatible. He has also recently included Poly and Diffusion fill in the standard cells, so that designs create by automatic Place and Route will satisfy the Fill rules. This appears to work well for the blocks checked so far (some M2 and M3 fill may be needed, depending on the routing density in the design).
- Although RAL will be updating this library, we have agreed to keep this frozen version for this generation of chips.

Pad Frame:

- Peter Denes has been working on an improved set of pad designs. These incorporate better ESD protection than the pads in the present RAL design kit (they have only small diodes on digital inputs, and no protection on output pads or power pads). They also incorporate an improved pad design recommended by TSMC (arrays of vias in particular pattern) and are TSMC compatible.

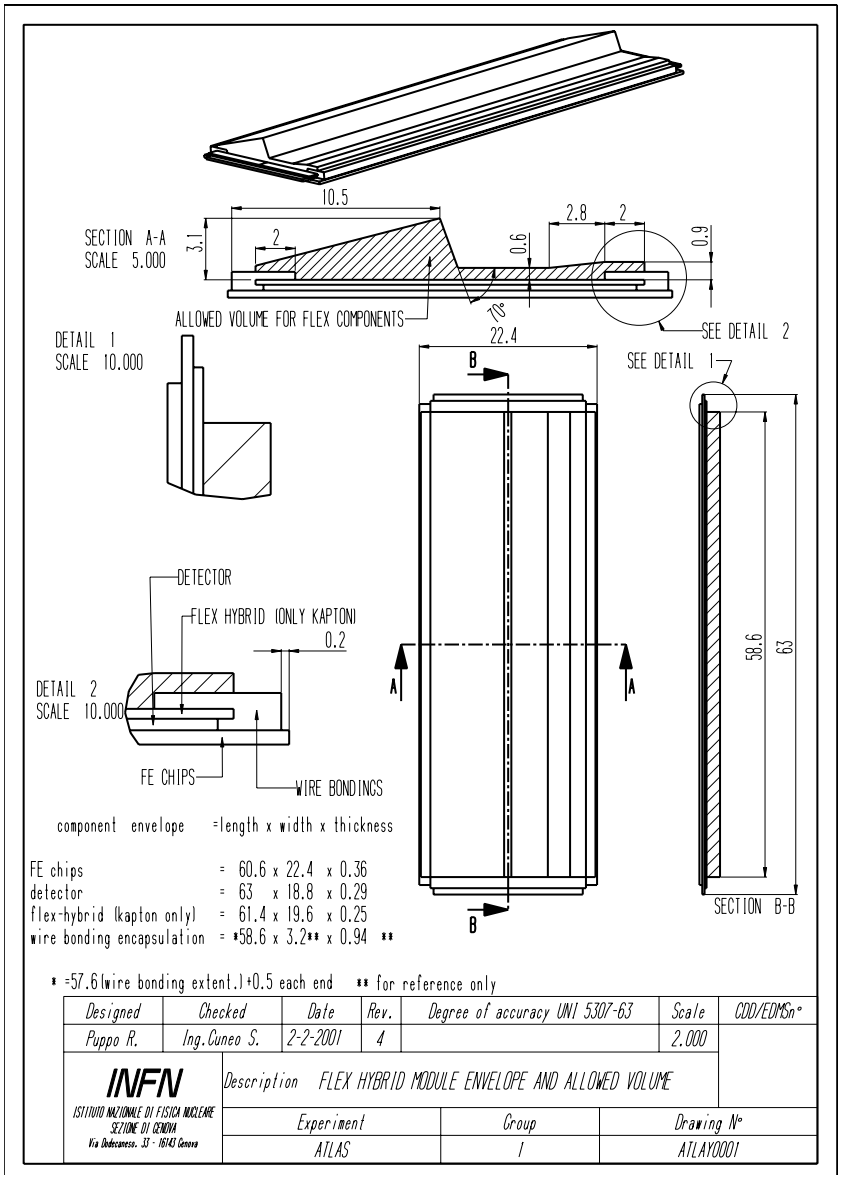


Pad has 95μ square opening. Final pad is likely to be 95μ x 150μ, or perhaps even as large as 95μ x 200μ, to allow multiple re-bonding attempts.

- There are already CMOSIn, CMOSOut, VDD, and VSS pads. The LVDS I/O pads are under development, with core schematics by Laurent, and layout by Bonn. The core will be included in a pad-pair frame of the type described above.
- These pads will be used for the Feb/Mar submissions.

Module Envelope and Wire-Bonding Constraints

Summarize constraints on module envelope:



Constraints on FE die size:

- Present prototypes use: 7.2x(8.0+2.8)mm design size with 0.1mm dicing zone all around: 7.4x11.0mm as-cut die size.
- Production size agreed to be same: Provides total chip envelope in z of 8*7.4 + 7*0.2 = 60.6mm

Constraints on FE bonding region:

- End chips have a constraint on the region which may be wire-bonded, in order to provide good Z overlap. Bonds must fit in central 57.6mm of module, meaning central 4.4mm out of the 7.4mm as-cut die width.
- If we retain the present 150μ bond-pad spacing, that corresponds to 30 bonding pads (4.35mm + pad size).

Proposed Final FE Chip Pinout (30 bonded pads):

- Total of 10 power pins, positioned at 1/4 and 3/4 points in die (mirrored) :

  p11, p38 VDDA
  p12, p37 AGnd
  p13, p36 Shield
  p14, p35 DGnd
  p15, p34 DVdd

- Total of 1 analog pin (intended largely for lab calibration at this time):

  p20 VCal

- Total of 9 Command and Address pins:

  p16 - p19 GA0 - GA3
  p21 CCK
  p22 DI
  p23 LD
  p24, p25 STRn, STRp

- Total of 6 control pins:

  p26, p27 SYNCn, SYNCp
  p28, p29 XCKn, XCKp
  p30, p31 LV1n, LV1p

- Total of 2 output pins

  p32, p33 DOn, DOp

- Total of 2 detector pins:

  p10 DGuard
  p39 DGrid

To reach this, have removed 18 pads from present pinout:

- RSTb, and Analog pins (I1-I8, and VCCD/VTH)
- All monitoring pins (MonHit, MonSel, MonRef, MonAmp)
- Propose to retain most on the die, in locations compatible with present floorplans:
- Total of 1 control pin:

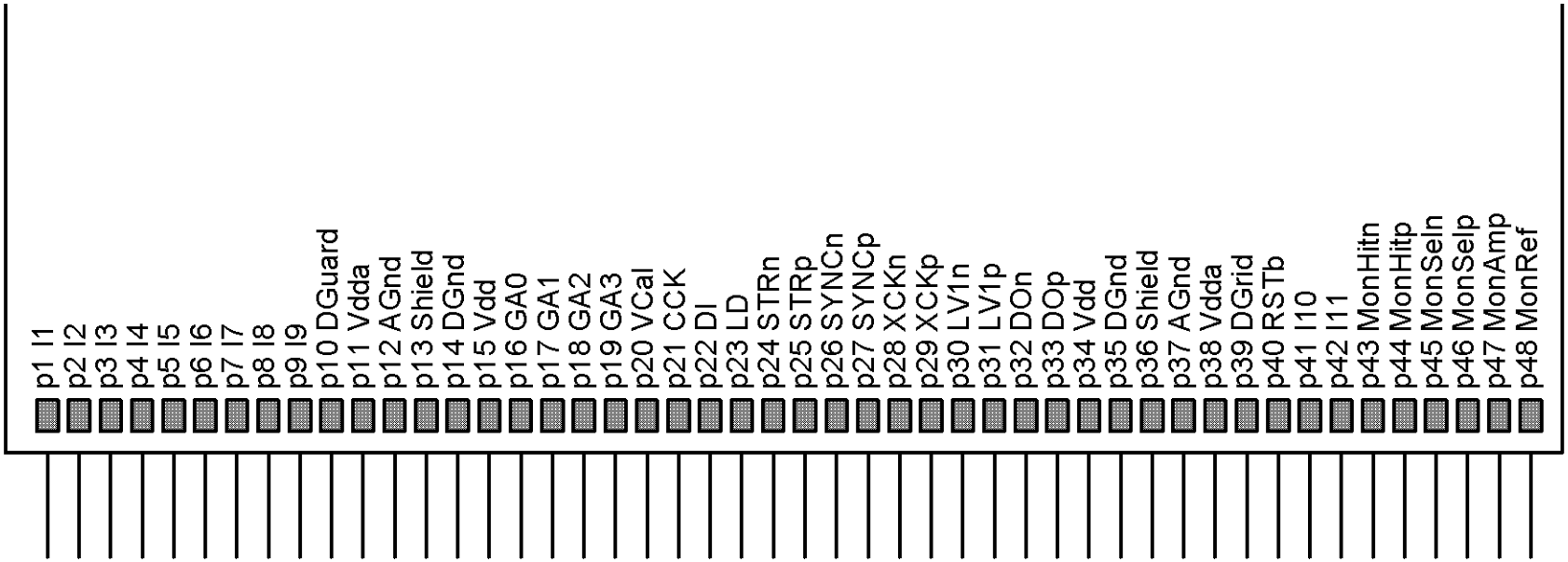
  p40 RSTb
- Total of 11 current monitor pins (may not all be used):

  p1 I1
  p2 I2
  p3 I3
  p4 I4
  p5 I5
  p6 I6
  p7 I7
  p8 I8
  p9 I9
  p41 I10
  p42 I11
- Total of 6 special monitoring pins:

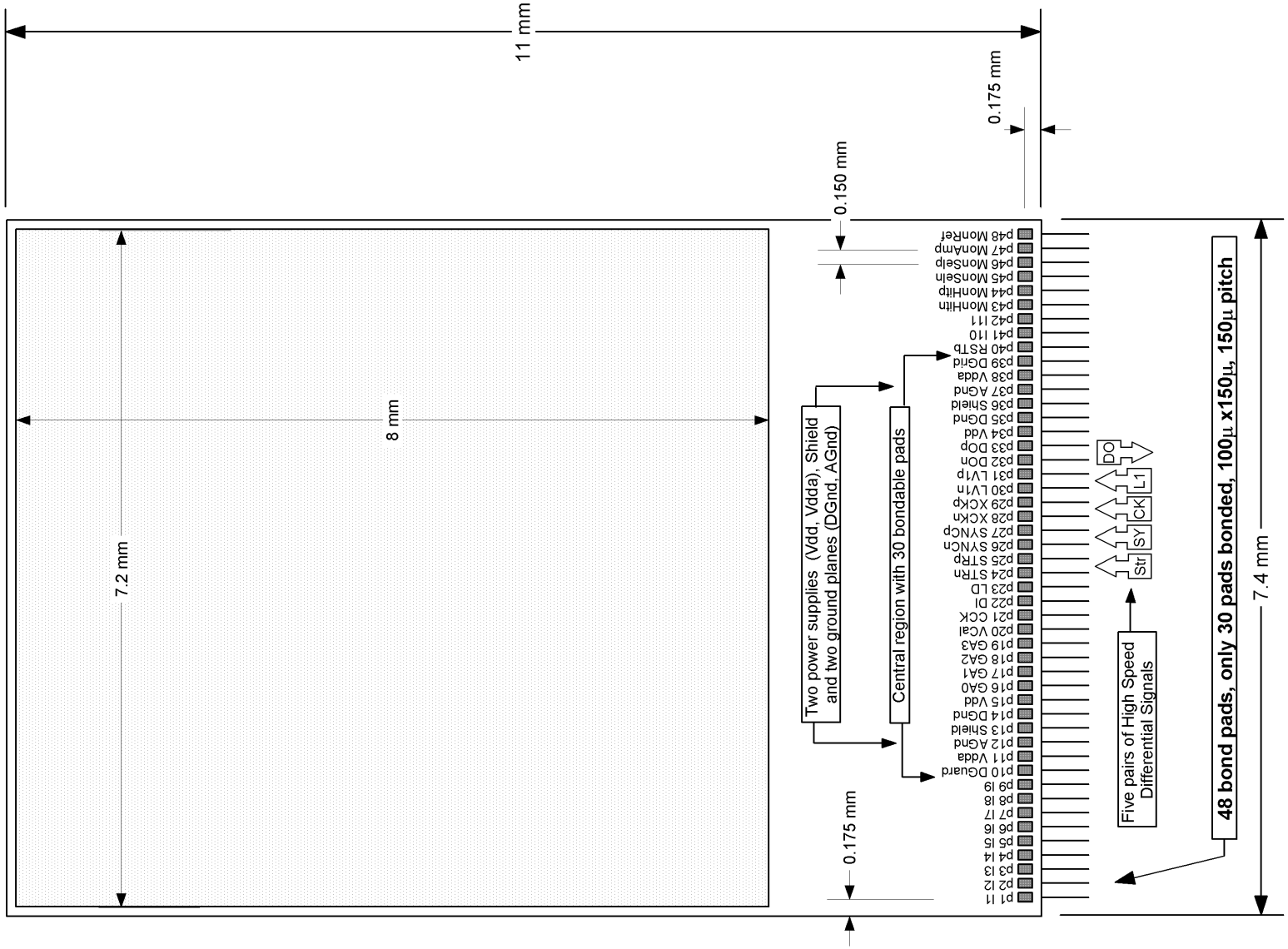
  p43, p44 MonHitn, MonHitp
  p45, p46 MonSeln, MonSelp
  p47 MonAmp
  p48 MonRef

Proposed Pad Geometry:

- Increase present pad size to 100µ x 150µ rectangle, with 150µ pitch, to provide more pad area for rebonding. Include MCM-D bump-bondable I/O pads with the same geometry used in FE-D (relative to the bottom of the wire bond pads).
- Continue to locate pads close to the lower die edge, as for demonstrator chips.
- The present demonstrator geometry has 48 pads, with centers along a line 175µ above the bottom (referenced to the as-cut die size of 7.4x11.0mm). The first pad center is also 175µ from the vertical edge referenced to the as-cut die size.
- Propose that this pad placement would be retained, and only the central 30 pads would be used for production bonding:



Overall Chip Geometry:



Further modifications that could be considered:

- Could reduce pads further by reducing to single power connections. This is probably possible given the internal voltage drops achievable in the 0.25µ processes, but reduces redundancy. This would require power pads to be located in the center of the chip. The redundant bond connections seem particularly important for the digital supply to avoid a single missing wire-bond killing a whole module.
- Could further reduce the extra pads by MUXing many current DACs through a single monitoring pin.
- In order to make an appreciable gain in pad pitch as far as the Flex technology is concerned, would need to go to 200µ pitch. This would reduce the number of bondable pads from 30 to 23, which is difficult to achieve in this pinout. Eliminating one set of power connections completely, plus VCal, is only six pins.

Test Chip Program

Take advantage of frequent runs, rapid turnaround of TSMC:

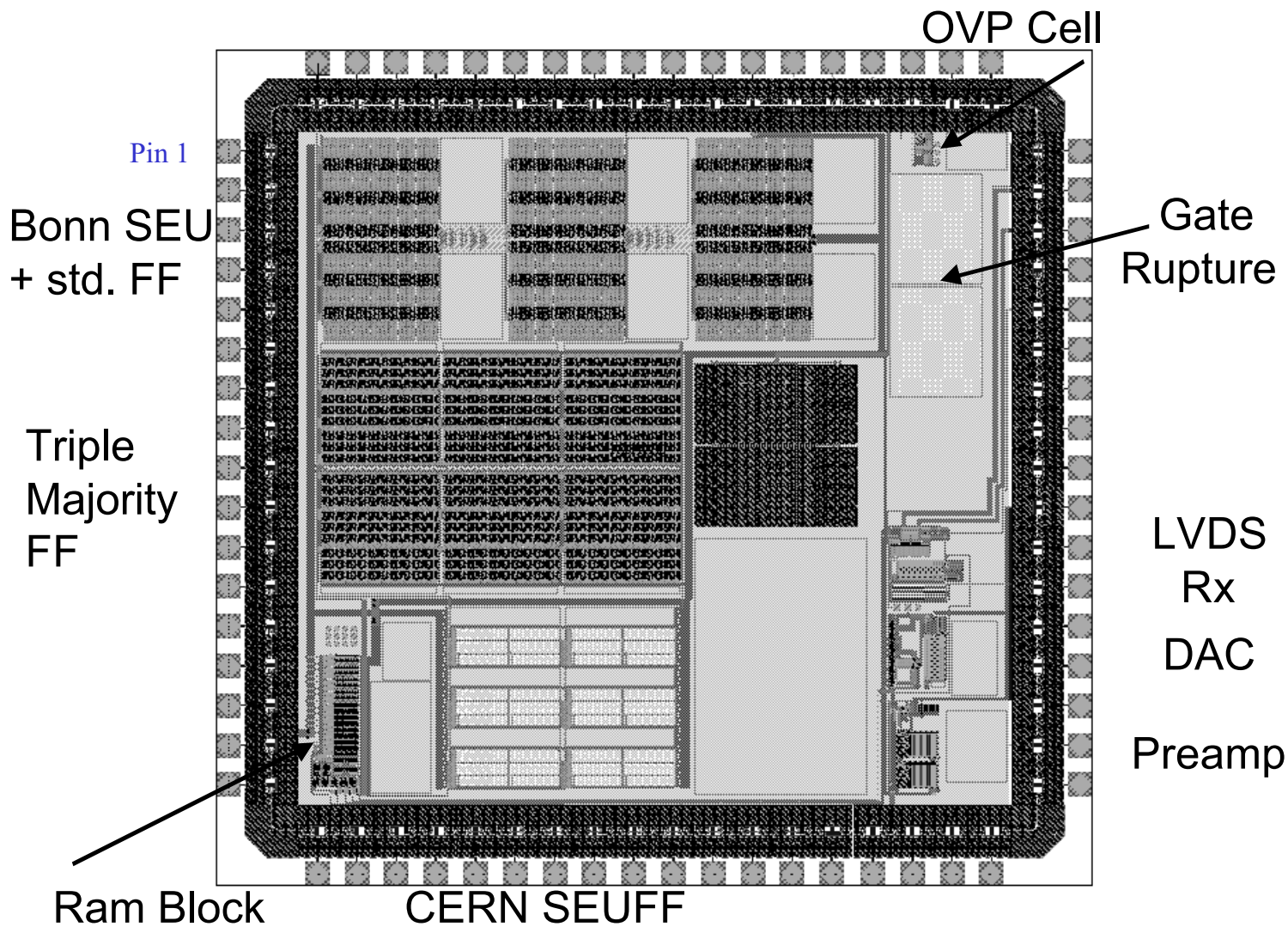
- Earliest date for useful submission was Jan 8.
- Goal of the initial submission was to include several of basic blocks from FE-I, and evaluate their performance.
- Check that we understand design rules, agreement of performance with SPICE, and behavior during irradiation (SEU) and post-rad (total dose) is as expected.

List of blocks included:

- Current reference and current DAC used in bias control.
- Redesigned LVDS driver and receiver blocks (only driver included).
- Pixel RAM block with 32 memory locations and sense amplifier readout.
- Several basic shift registers, for evaluation of SEU performance. Designs included: standard cell version, CERN SEU-tolerant version, improved Bonn SEU-tolerant version, and three-fold majority logic version.
- Preamp test block with first version of preamplifier design.
- Miscellaneous test structures for gate rupture, and other ideas.

A small chip of 12mm^2 was submitted at 13:00 on Jan 8.

The test chip submitted:



- Chip has 70 pins and the die size was basically pad-limited.

Details of some interesting blocks:

- SR blocks are 6 groups of 13 bits, or 78 bits total.
- Pixel RAM block has Read line to control whether external 8-bit TSI data is written or read from RAM array. One of the TSI inputs is differential for timing tests. A 4-bit ADDR MUX is used to select the location for reading/writing LE/TE data. Sixteen sense amps are used to read the data back and send it to the output pads.
- Preamp block has all bias inputs available as external pins, plus 50ohm buffer for looking at the output pulse shape.

Post-mortem:

- Due to the timing of the submission over the holidays, and the absence of key personnel for family reasons, we were not able to properly LVS the chip before submission. All of the individual blocks were LVSed. There were several minor DRC errors. At the time, this seemed an acceptable risk for a first submission.
- After experts returned, real checking began. It turns out that there were a number of errors in the chip.
- Nevertheless, with minor FIB surgery, we believe it will be possible to obtain some useful results from the chip, although much less than we had hoped.
- **Estimated wafers out date advanced to Feb 27 (8.6 weeks turn-around !)**

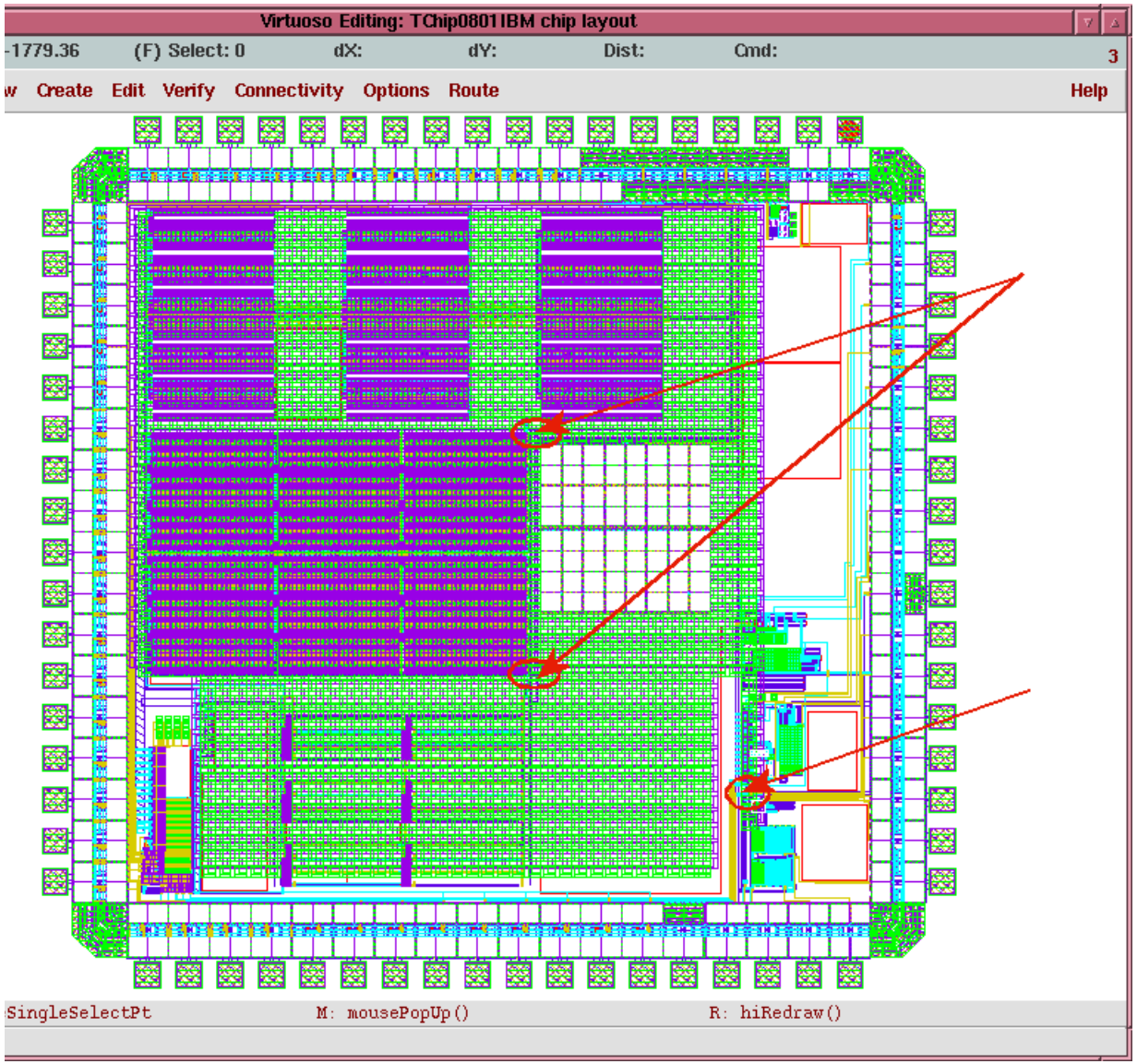
List of known major errors for Jan 8 submission:

- Internal shorts between VDD and GND in the triple redundancy FF chain, which require its supply lines to be cut in order to operate the chip. This was due to an incorrect understanding of Cadence LVS procedure.
- Floating gates on protection diodes in analog pads. This occurred because of recycling of hierarchical digital pad design, and then forgetting to add top layer properly. This effectively kills all access to the analog blocks in the test chip (preamp, reference, DAC).
- Probe pads for testing DAC control register shorting VDD and GDD to output of shift register.
- Error in connecting power supplies to DAC register, resulting in VDD and GND being shorted. As this block operates on the digital supply, this short (single trace) must be cut to allow powering the test chip.
- Power supply short in LVDS driver due to misplaced power connection.

Proposal for testing:

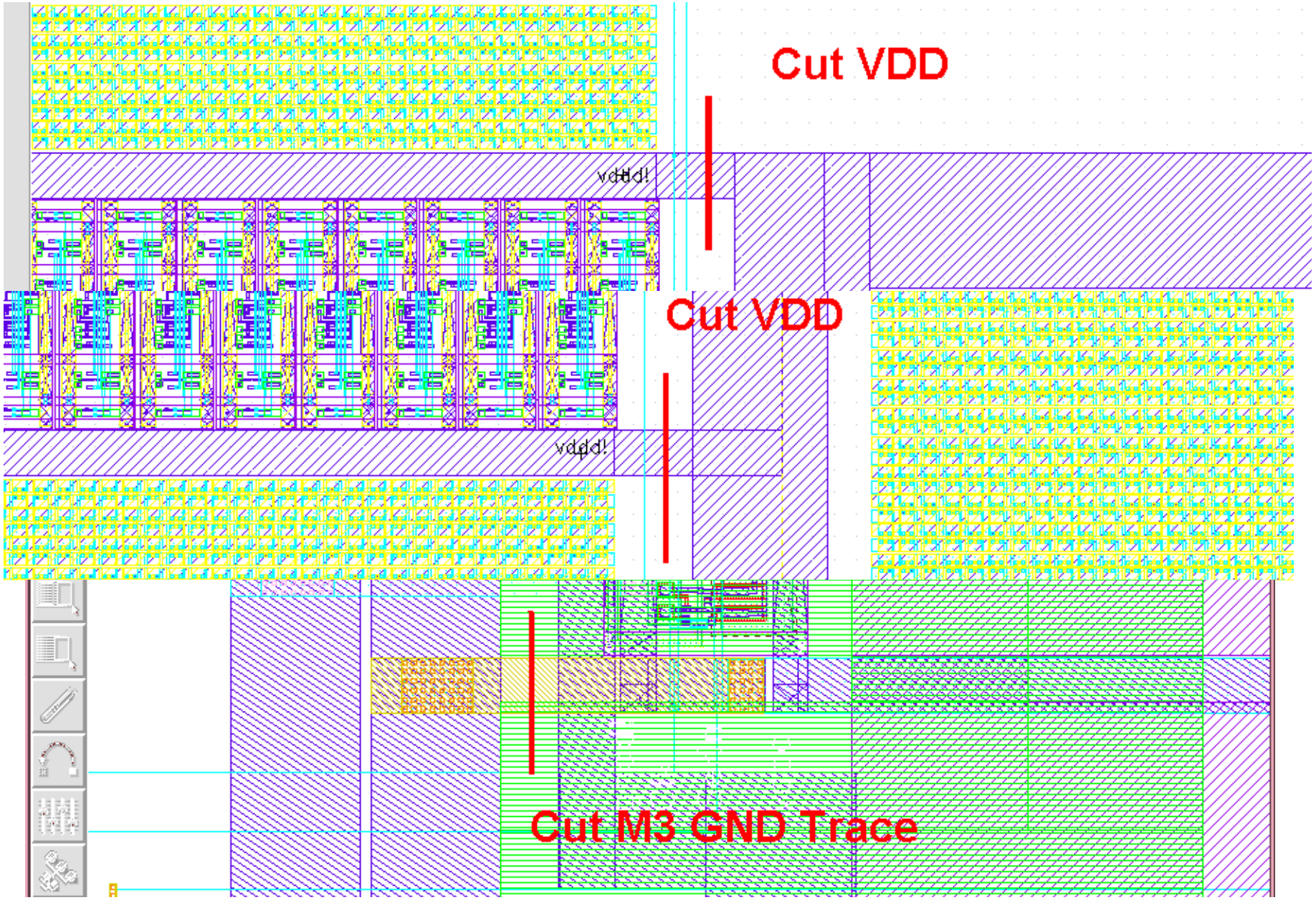
- Cutting three traces using FIB should allow application of digital power, and testing of 3 shift register blocks (standard cell, Bonn SEU-tolerant, and CERN SEU tolerant) plus the Pixel RAM block.
- There seems to be little hope for testing analog blocks without vast FIB effort.

FIB Modifications to resurrect the test chip:



- Arrows indicate approximate locations of three traces where cuts are required to eliminate shorts on digital VDD.
- Two leftmost cuts isolate triple FF from VDD, rightmost cut eliminates VDD/GND short near DAC
- Have verified that making these cuts elimates all shorts between digital VDD and GND.

Detailed plots of modifications:



Next Steps in Test Chip Program:

- Originally planned to make second TSMC submission on Feb. 5. This was to be the equivalent to the Analog Test Chip prepared by Peter Fischer for the DMILL runs. We were not adequately ready for this date, and have postponed.
- Meanwhile, CERN has significantly tightened their MPW submission rules with the goal of more reliable turn-around dates (now claim possibility, but not guarantee, of 12 week turnaround), and has added a second April run. Given this, we decided to participate in the Feb IBM MPW with a 16mm^2 die, in the hopes that we might receive the test chips by June 1. Note this is a 3M run only, so some modifications from the full test chip are required.
- We intend to also send this test chip to TSMC on Mar 5.
- These two submissions should give us significant feedback on fairly final aspects of our analog design in middle to late May if turn-arounds are good.
- These submissions are all being financed by remaining special US money originally earmarked for the FE-H submission, and total cost for all three test chip submissions should be about 50K$.
- More details of designs being included in this submission are described in talk from Peter Fischer.

Milestones in overall schedule:

- Some slippage over original very aggressive June 1 schedule, but believe this can be limited to a few weeks. Critical phase will be verification, which is largely still to come.
- Submission should still be during June (we have reserved a run during Q201, and if we slip beyond this, there will be a 30K$ penalty to submit in Q301).
- In order to get the guaranteed turnaround, the design would need to be DRC-clean, requiring us to begin foundry-level DRC checking (using Hercules) at least several weeks earlier.
- We are already running the Dracula DRC for IBM, but we have discovered that the rule set is not complete (ESD rules missing). Will make comparisons with Hercules soon we hope.
- Worst case thirteen week turnaround in the frame contract would give wafers during the month of September. This might allow some testbeam and irradiation studies at CERN before shutdowns in early November. Most optimistic schedule would be an 8 week turn-around, that would give wafers during August.